REMARKS

Claims 1-7 and 9-67 are pending in the application. Claims 1, 25, 28, 29, 52, 65 and 66 are independent claims. Claims 1-7, 9-26, 28-42, 44-50, 52-63 and 65-67 stand rejected. Claims 27, 43, 51 and 64 stand objected to.

Claim Rejections – 35 USC § 103(a)

Claims 1-5, 7, and 17-21 stand rejected under 35 U.S.C. 103(a) as being unpatentable over John Scott Robin (*Analyzing the Intel Pentium™'s Capability to Support a Secure Virtual Machine Monitor, pp 1-98, Sep., 1999, Naval Postgraduate School, Monterey, California*) (hereafter 'Robin') in view of Devine et al. (Pat No. 6,397, 242 B1) (hereinafter 'Devine') and Bennett et al. (Pat. No. 7,127,548 B2) (hereinafter 'Bennett' – art made of record).

Applicants respectfully disagree and traverse the rejection.

Regarding the rejection of claim 1, The examiner maintains the Robin discloses the problem of implementing secure virtual machine monitors (VMM) on the Intel Pentium Architecture and presents techniques that allow the Intel Architecture to support a "virtual VMM." The examiner admits, however, that Robin does not explicitly disclose synthetic instructions that cause at least one exception to be trappable by a virtualization layer, wherein said synthetic instructions are illegal to said architecture. For that element of the claim, the examiner relies on Devine.

The examiner maintains that Devine discloses synthetic instructions by citing various sections of Devine:

> (e.g., Abstract, . .. Connected to the VMM for running a sequence of VM instructions . . .) that cause at least one exception (e.g., Col. 8, Lines 35-43 - ... Can be changed only by protected mechanisms, either instructions or exceptions; Col. 12, Lines 57-60 - ... if the execution of the instruction leads to an exception of the virtual machine ....; Col. 14, Lines 57-60 - . . . requirements of the virtual machine monitor . . . . is the ability to handle traps (exceptions and interrupts) transparently to the execution of the virtual machine) to be trappable (e.g., Col. 2, Lines 2-4 - the VMM thus need only to correctly emulate the traps to allow the correct execution of the operating system in the virtual machine; Col. 4, Lines 52-54 - .

> .. the VMM must handle only the traps that result from attempts by the virtual machine to issue privileged instructions) ….

Action pp. 4-5. Applicants respectfully disagree that the cited teachings of Devine meet the claim limitations. Devine simply does not teach the synthetic instructions as claimed. First, the claim requires that the operating system instructions are modified. Devine doesn't teach that. Moreover, the claim requires the modification to occur through the use of "at least one synthetic instruction." Devine teaches binary translation and not the use of synthetic instructions. Synthetic instructions cause "at least one exception to be trappable by a virtualization program" and are also "illegal to said architecture." The same cannot be said of the system of Devine. Devine does not remove, replace or supplement guest operating instructions with instructions that are "illegal to said architecture." On the contrary, Devine uses binary translation to present instructions that can be executed on the specific architecture. This element of the claim is clearly not present in Devine. For that reason alone, Applicants submit that claim 1 patentably defines over Devine.

Inasmuch as claims 2-5, 7, and 17-21 depend from claim 1, Applicants submit that they also patentably define over Devine for at least the reasons state with respect to claim 1.

Claims 29, 34-37, 44, 52, and 57-60 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Bennett. Applicants respectfully disagree and traverse the rejection.

Regarding claim 29, the examiner maintains that Robin teaches:

> ***a subsystem for trapping said synthetic instructions*** issued by a guest operating system after said synthetic instructions cause an exception in the x86 processor; and a subsystem for processing said synthetic instructions for the guest operating system (i.e. P. 5, Sec. 3 – Logical VMM Modules -A VMM normally has three generic types of modules: dispatcher, allocator, and interpreter; A jump to the dispatcher is placed in every location to which the machine traps. The dispatcher then decides which of its modules to call when the machine traps; For example, if a VM tries to execute a privileged instruction that would change the resources of the VM's environment, the VM will trap to the VMM dispatcher. The dispatcher will handle the trap by invoking the allocator that performs the requested resource allocation according to VMM policy. The final module type is an interpreter. Each privileged instruction

> will have an interpreter module that is called by the dispatcher
> to simulate the effect of the instruction that caused the trap)

Action p.29. As indicated above with respect to claim 1, Applicants submit that Robin simply does not teach the use of synthetic instructions as claimed. For that reason alone, Applicants submit that Robin alone of in combination with Bennett do not render the claim obvious. Reconsideration is respectfully requested.

Inasmuch as claims 34-37 and 44 depend from claim 29, Applicants submit that they also patentably define over Devine for at least the reasons state with respect to claim 1.

Regarding the rejection of claims 52, and 57-60, Applicants submit that they are patentable for at least the reasons with respect to claims 1 and 29.

Claims 33 and 45 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Bennett and Devine.

Inasmuch as claims 33 and 45 depend from claim 29, Applicants submit that they also patentably define over Devine for at least the reasons state with respect to claim 1.

Claim 65 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Devine.

As indicated above with respect to claim 1, Applicants submit that neither Robin nor Devine teach the use of synthetic instructions as claimed. For that reason alone, Applicants submit that Robin alone of in combination with Devine does not render the claim obvious. Reconsideration is respectfully requested.

Claim 28 stands rejected under 35 U.S.C. 103(a) as being unpatentable over K. Virtual 8080 Mode (*Intel 80386™ Programmer's Reference 1986, pp. 1-18, 1986, Intel 80386™ Programmer's Reference*) (hereinafter 'V86') in view of Devine and Bennett.

As indicated above, neither Devine nor Bennett teach synthetic instructions as claimed. The examiner now further cites V86 for the following proposition:

> replacing the trappable instructions with corresponding syntheticinstructions that are at least five bytes long (e.g., PP. 10-1 1, "Additional Sensitive Instructions", CLI - Clear

> Interrupt-Enable Flag; ST1 – Set Interrupt-Enable Flag; PP. 1 1-1 2, "Virtualizing the Interrupt-Enable Flag", 1 Para - 2" Para)

Action p. 32. However, it makes no sense that V86 teaches synthetic instructions when the claim recites that "synthetic instructions are illegal to a physical processor architecture underlying said guest operating system." For at least the foregoing reason, Applicants submit that claim 28 patentably defines over V86 in view of Devine and Bennett.

Claim 67 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Devine in view of Bennett. Applicants respectfully disagree.

Claim 67 recites:

> 67. A method for processing synthetic instructions executable on a processor architecture, comprising:
>
> removing, replacing, or supplementing at least one predefined instruction in a guest operating system, running in a virtual machine environment, with synthetic instructions;
>
> determining whether said synthetic instructions are supported by said virtual machine environment by executing at least one of said synthetic instructions;
>
> enabling direct execution of instructions on said processor architecture using at least one of said synthetic instructions;
>
> wherein at least one of said synthetic instructions is configured to cause at least one exception trappable by a virtualization layer when privileged-level code is run at user-level, wherein at least one of said synthetic instructions is illegal to said processor architecture;
>
> causing said at least one exception to be issued by said processor architecture by using at least one of said synthetic instructions;
>
> invoking a trap handler within said virtualization layer in order to trap said at least one exception;
>
> emulating with said virtualization layer any implied state changes based on processing of said at least one exception; and
>
> returning control to any subsequent instructions of said guest operating system.

As indicated repeatedly above, Devin simply does not teach synthetic instructions nor does it teach removing, replacing, or supplementing at least one predefined instruction in a guest operating system. At best Devine teaches binary translation that translates instructions into a form that the physical processor can execute. Bennett does not cure the deficiency of Devine.

Accordingly, Applicants submit that claim 67 patentably defines over Devine in view of Bennett.

Claim 25 stands rejected under 35 U.S.C. 103(a) as being unpatentable over K. P. Lawton (Bochs x86 Emulator – monitor-host.c, pp. 1-42, bochs.sourceforge.net) (hereinafter 'Lawton') in view of Devine and Bennett.

As an initial matter, Applicants note the examiner cites section 102(a) on page 38. Applicants assume this is an error because a 103(a) analysis is applied in the rejection.

As previously pointed out, neither Devine nor Bennett teach the claim limitation of:

> wherein said synthetic instructions are configured to cause at least one exception to be trappable by a virtualization layer, and wherein said synthetic instructions are illegal to said processor architecture

Lawton fails to cure this deficiency as noted by the examiner on page 40 of the Action. Consequently, Applicants submit that claim 25 is patentable over the cited references.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lawton in view of Devine and Robin.

Inasmuch as claims 26 depends from claim 25, Applicants submit that it also patentably define over Lawton in view of Devine and Robin for at least the reasons state with respect to claim 25.

Claims 15-16 and 22-23 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Devine, Bennett and V86.

Inasmuch as claims 15-16 and 22-23 depend from claim 1, Applicants submit that they also patentably define over Robin in view of Devine, Bennett and V86 for at least the reasons state with respect to claim 1.

Claims 31-32, 38-39, 46-48, 55-56 and 61-62 stand rejected under 35 U.S.C. 102(a) as being unpatentable over Robin in view of Bennett and V86.

Inasmuch as claims 31-32, 38-39, 46-48, 55-56 and 61-62 depend from claims 29 and 52, Applicants submit that they also patentably define over Robin in view of Devine, Bennett and V86 for at least the reasons state with respect to claims 29 and 52.

Claim 13 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Devine and Bennett and further in view of Lawton.

Inasmuch as claim 13 depends from claim 1, Applicants submit that it also patentably define over Robin in view of Devine, Bennett and further in view of Lawton for at least the reasons state with respect to claim 1.

Claims 41-42, 54, and 63 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Bennett and Lawton.

Inasmuch as claims 41-42, 54, and 63 depend from claims 29 and 52, Applicants submit that they also patentably define over Robin in view of Bennett and Lawton for at least the reasons state with respect to claims 29 and52.

Claim 14 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Devine and Bennett and further in view of Carlos et al. (*User-Kernel Reactive Threads for Linux, Jan. 2003, SCI 2003, pp. 1-6*) (hereinafter 'Carlos').

Inasmuch as claim 14 depends from claim 1, Applicants submit that it also patentably define over Robin in view of Devine and Bennett and further in view of Carlos for at least the reasons state with respect to claim 1.

Claims 30 and 53 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Bennett and Carlos.

Inasmuch as claims 30 and 53 depend from claims 29 and52, Applicants submit that they also patentably define over Robin in view of Bennett and Carlos for at least the reasons state with respect to claims 29 and 52.

Claims 6, 9 and 24 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Devine and Bennett and further in view of Cota-Robles et al. (Pat. No. US 7, 191,440 B2) (hereinafter 'Cota-Robles')

Inasmuch as claims 6, 9 and 24 depend from claim 1, Applicants submit that they also patentably define over Robin in view of Devine and Bennett and further in view of Cota-Robles for at least the reasons state with respect to claim 1.

Claim 40 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Bennett and further in view of Cota-Robles.

Inasmuch as claim 40 depends from claim 29, Applicants submit that it also patentably define over Robin in view of Bennett and Cota-Robles for at least the reasons state with respect to claim 29.

Claim 49 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Bennett and V86 and further in view of Carlos.

Inasmuch as claim 49 depends from claim 29, Applicants submit that it also patentably define over Robin in view of Bennett and V86 and further in view of Carlos for at least the reasons state with respect to claim 29.

Claim 50 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Bennett and V86 and further in view of Lawton.

Inasmuch as claim 50 depends from claim 29, Applicants submit that it also patentably define over Robin in view of Bennett and V86 and further in view of Lawton for at least the reasons state with respect to claim 29.

Claim 66 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Lawton, Carlos and further in view of V86.

Applicants respectfully disagree. The examiner maintains that Lawton teaches replacing CPUlD instructions in the guest operating system with synthetic instructions. Action p. 80. However, as noted above, Lawton does not teach the use of synthetic instructions as claimed.

For at least the foregoing reason, applicants submit that claim 66 patentably defines over Robin in view of Lawton, Carlos and further in view of V86.

Claim 10 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Robin in view of Devine, Bennett and A. Tamches (*Fine-Grained Dynamic Instrumentation of Commodity Operation System, May, 2001, University of Wisconsin -Madison*) (hereinafter 'Tamches').

Inasmuch as claim 10 depends from claim 1, Applicants submit that it also patentably define over Robin in view of Devine, Bennett and A. Tamches for at least the reasons state with respect to claim 1.

Claims 11-12 stand rejected under 35 U.S.C. 102(a) as being unpatentable over Robin in view of Devine, Bennett and Tamches and further in view of V86.

Inasmuch as claims 11-12 depends from claim 1, Applicants submit that it also patentably define over Robin in view of Devine, Bennett and Tamches and further in view of V86 for at least the reasons state with respect to claim 1.

Allowable Subject Matter

Applicants thank the examiner for acknowledging the patentability of claims 27, 43, 51 and 64. In view of the foregoing amendments and arguments, Applicants submit that all of the claims remaining in the application are allowable.

CONCLUSION

In the view of the foregoing amendments and remarks, Applicants respectfully submit that the present application is in condition for allowance. Reconsideration of the application and an early Notice of Allowance are respectfully requested. In the event that the Examiner cannot allow the application for any reason, the Examiner is encouraged to contact Applicants' representative.

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